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Literature Review on High Frequency Affects and Methodologies in Reduction of EM Interference and IR Drop in VLSI Circuits

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Abstract: This paper presents the literature review on electromagnetic interference, and power leakage minimization. To reduces the EM interference and IR drop by using various methodologies applied by researchers. For any research work or in an effort to introduce certain novelty in existing systems, the analysis and study of existing approaches, systems and algorithms is of great significance. In fact, the review of existing systems can be stated to be the foundation for a novel research. Thus, taking into consideration of these requirements to examine and study varies literatures available for the impact of my work carried out on Electromagnetic interference on VLSI and IR drop, power dissipation and performance of chip, in this paper a number of literatures have been studied and analyzed.

Key words: EMI, EMC, IR drop, SOC, VLSI, Ldi/dt, CMOS, DSM.

I. INTRODUCTION

This paper discusses some of the relevant and significant researches conducted and associated literatures discussion voltage drop and IR drop issues in high speed semiconductor or VLSI device design. In addition, a number of literatures discussing electro migration, IR drop analysis with both static as well as dynamic analysis etc have been discussed. Researchers in their work discussed varied aspects of EMI in SOPs, such as die/package-level EMI, substrate-level EMI, electromagnetic modeling and simulation; and near electromagnetic field measurement. Researchers in their work, at first studied the LSI designs in association with the radiated emission, where they found that the signal-return path loop and switching current in the power/ground line are inherent sources of EMI. Researchers found that maintaining the return current path is an important aspect of substrate design for suppressing EMI and for maintaining signal integrity (SI) Ordinarily in SOPs, high-performance digital LSIs are sources of EMI, while RF and analog circuits are affected by EMI (victims).. Furthermore, isolating and suppressing the resonance of the DC power bus in a substrate is another important design aspect for EMI and for power integrity (PI).

II. LITERATURE REVIEW

Jiang et al [1] addressed the issue of analyzing the performance degradation caused by noise in power supply lines for deep submicron CMOS devices. Researchers proposed a statistical modeling technique for the power supply noise including inductive ΔI noise and power net IR voltage drop that was further integrated with a statistical timing analysis. Their experimental results exhibit that on average, with the consideration of this noise effect, the circuit critical path delays increase by 33% and 18%, respectively for circuits implemented on these two technologies..Sinha et al [2] stated that for high-speed circuits, on-chip inductance can no longer be ignored. Researchers dealt with the inductance in the presence of multilayered meshes used for on-chip power supplies. In their work, they explored approaches to design power/ground (p/g) mesh that might reduce inductance. Challenging the development of an accurate 3-dimensional inductance extraction for large chips, they demonstrated the feasibility of using flexible-accuracy empirical formulae for fast determination of inductance in chips. Cui et al [3] stated that the increasing speed of digital circuit design as well as the density of printed circuit board (PCB) layouts often result in more challenging electromagnetic interference (EMI) problems. The coupling between a high-speed digital line and an I/O line can be a primary EMI coupling path, and the attached cable a dominant radiator. They developed a multi-stage modeling approach where the EMI modeling was developed for coupling between the transmission lines, and the attached cable as the EMI antenna. Finally, the EMI was estimated for the coupled noise driving the attached cable. The agreement between the modeled and measured results demonstrated that the modeling method can be a suitable scheme for estimating the EMI due to high-frequency coupling to I/O lines.Wei et al [4] stated that for high-speed signals that transition through the internal parallel planes comprising the DC power bus, the return current has to switch from one reference plane to another reference plane. The return current discontinuity excites the DC power bus that might result in a power bus noise problem, as well as an EMI problem. Researchers studied EMI factors resulting from the signal transitions

through a DC power bus. They examined EMI resulting from the excited DC power bus and the effects of local and global decoupling as an EMI mitigation approach were also studied by researchers. In addition, researchers studied the noise coupled to I/O lines, and EMI for a test board with varying layer thickness between the power and ground planes. Zheng & Tenhunen [5] studied the power and ground distribution and its noise effect for deep submicron CMOS VLSI circuits. Researchers found that orders of magnitude reduction in switching noise can be achieved using an effective power and ground distribution scheme. Kimothi et al [6] discussed how the uncertainty factor impacts on the product characteristics in the manufacturing organisation or testing laboratories. Researchers stated that the compliance decision has to take the uncertainty factors into consideration. In their manuscript, researchers described how these factors are considered for judging compliance for electromagnetic interference/electromagnetic compatibility (EMI/EMC) and safety.. Shiyou & Roy [7] scaled down the transistor dimensions aggressively while lower power dissipation is achieved by scaling down the supply voltage so as to for achieving high performance and high integration density. Author stated that power distribution has become a challenging issue due to the severe switching noise on the power distribution network and hence estimation of the worst case switching noise is essential to ensure the proper functionality of the VLSI circuits. Author stated that the switching noise can be suppressed effectively with properly placed decoupling capacitors, In order to achieve these, researchers proposed a probabilistic approach to determine the lower bound of the worst case switching noise on power supply lines where the proposed algorithm traces the worst case input patterns which induces the steepest maximum switching current spike and therefore the maximum switching noise. The worst case input patterns were used in the HSPICE simulation so as to extract the exact switching current waveforms where the estimated maximum switching current spike matches well with the peak current obtained from the HSPICE simulation. The magnitude of the worst case switching noise for the benchmark circuits implemented with 0.25 μm technology can be as high as 35% of the V_{dd}. Resve et al [8] stated in their research that clocks are perhaps the most important circuits in high-speed digital systems and hence the design of clock circuitry and the quality of clock signals directly impact the performance of a very large scale integrated chip. Clock skew verification requires high accuracy and is typically performed using circuit simulators. The effect of IR-drop on the timing of clock signals was quantified on a small example, and demonstrated on a large chip. Sasaki et al [9] presented a new decoupling circuit for multi-power-terminal VLSIs to suppress strong radiated emissions caused by power plane resonance of multilayer printed circuit boards (PCBs). Their circuit was based on a previous π-network filter consisting of two capacitors and one power trace. The power trace, designed in agreement with transmission line theory, was used in place of the ferrite bead inductor of a conventional π-network filter. The new circuit has been so designed that when a number of them are applied in combination to a multi-power-terminal VLSI, they can share capacitors, thus reducing the total number of capacitors required. Both calculated and measured high-frequency characteristics of power buses in PCBs exhibited that in wide-band frequencies their proposed circuit can potentially isolate a VLSI, the source of switching noise, from power distribution buses, which might otherwise resonate that switching noise. Wei et al [10] discussed the signal vias and its application in multilayer printed circuit board (PCB) design. Researchers stated in their work that for a signal via transitioning through the internal power and ground planes, the return current has to jump from one reference plane to another reference plane. The discontinuity of the return current at excites the power and ground planes, and results in power bus noise that can produce an EMI problem. To deal with this situation, researchers employed approaches such as finite-difference time-domain (FDTD), moment methods (MoM), and partial element equivalent circuit (PEEC). Researchers investigated system performance towards the EMI mitigation by means of adding decoupling capacitors with the FDTD scheme. Steinecke et al [11] presented a set of design circuits and measures to improve EMC on silicon. They defined the range from RC low-pass noise filtering to improved I/O driver and clock distribution concepts. Their simulation results were demonstrated direct on-chip measurements and normative-compliant external emission measurements. Steinecke et al [12] discussed that significance of researches on effort on EMC models and simulation for chip design because of the high pace increase in the demands for reduced electromagnetic emission on chip-level in combination with more complex circuits and faster design cycles. In their research, authors developed a three-level approach, on the basis of: (1) test chip design and measurement; (2) RLC-extraction of supply system plus transistor net list simulation; and (3) behavioral models for simple gates and complex digital modules. Researchers observed and defined the correlation between results of their developed three levels and examined the behavioral models for complete CMOS VLSI chips. Kevin et al [13**]** analyzed simultaneous switching noise (SSN) which has emerged as one of the significant issues in the design of the internal on-chip power distribution networks in current very large scale integration/ultra large scale integration (VLSI/ULSI) circuits. Researchers employed an inductive model to characterize the power supply rails when a transient current is generated by simultaneously switching the on-chip registers and logic gates in a synchronous CMOS VLSI/ULSI circuit. In addition, researchers developed an analytical expression characterizing the SSN voltage on the basis of a lumped inductive-resistive-capacitive model RLC. Researchers found that the highest value of the SSN voltage based on this analytical expression exists within 10% as compared to SPICE simulations

Chen et al [14] explored about crosstalk effects and stated that crosstalk effects degrade the integrity of signals travelling on long interconnects. Researchers evaluated the performance of the system by implementing it test interconnects of a processor-memory system and the defect coverage was evaluated using a system-level

crosstalk defect simulation method. Nourani et al [15] developed a model for an integrity fault on the high-speed interconnects, where they presented a BIST-based test methodology that includes two special cells to detect and measure noise and skew occurring on interconnects of the gigahertz system-on-chips. Premkishore et al [16] examined the effect of technology scaling and micro architectural trends on the rate of soft errors in CMOS memory and logic circuits. They described and validated an end-to-end model that enables the computation of the soft error rates (SER) for existing and future microprocessor style designs. The model captures the effects of two important masking phenomena, electrical masking and latching window masking, which inhibit soft errors in combinational logic. Researchers' quantified the SER due to high-energy neutrons in SRAM cells, latches, and logic circuits for feature sizes from 600nm to 50nm and clock periods from 16 to 6 fan-out-of-4 inverter delays. They predicted that the SER per chip of logic circuits increases nine orders of magnitude from 1992 to 2011 and at that point will be comparable to the SER per chip of unprotected memory elements Shiyou et al [17] found that the peak power supply noise can be significantly reduced by judiciously arranging the modules based on their spatial correlations in the floorplan. Researchers in their work employed power supply noise as the cost function to determine the optimal floor plan in terms of area, wire length, and power supply noise. Compared to conventional floor planning, which only considers area and wire length, power supply noise aware floor planning can generate better floor plan both in terms of area and peak noise. The decoupling capacitance required by each module is also calculated and placed in the vicinity of the target module during the floorplanning process with 40%is reduced in both area and wire length.

Kao et al [18] suggested that to minimize total active power consumption in digital circuits, one must take into account sub threshold leakage currents that grow exponentially as technology scales. Researchers in their model developed a theoretical model to predict how dynamic power and subthreshold power must be balanced to give an optimal V_{DD}/V_t operating point that minimizes total active power consumption for different workload and operating conditions. Authors in their research developed a preliminary automatic supply and body biasing architecture (ASB) that automatically configures a circuit to operate with the lowest possible active power consumption. Grochowski et al [19] presented a novel technique to simulate power supply voltage variation as a result of varying activity levels within the microprocessor. Researchers in their work examined and discussed technique that can be implemented in logic on the microprocessor die to enable real-time computation of current consumption and power supply voltage. When used in a feedback loop, this logic makes it possible to control the microprocessor's activities to reduce demands on the power delivery system. With on-die voltage computation and di/dt control, they demonstrated that a significant reduction in power supply voltage variation may be achieved with little performance loss or average power increase. Harada et al [20] discussed the mechanism of radiated emission induced by traces placed between power/ground planes and analysed the radiation reduction techniques. Researchers found that the traces can cause voltage bounce between the power/ground planes and this bounce might result into high-level radiated emissions at resonant frequencies. Radiated emission characteristics predominantly depend on the trace location in the board; radiation level is high when the internal trace is located at a high voltage bounce area. Radiation reduction techniques were investigated where they found that the scattering of decoupling capacitors on the power distribution planes is not a useful technique to reduce the voltage bounce at higher frequencies. Thus, researchers suggested reduction in the voltage bounce narrowing space between these planes.Ohtsu et al [21] developed the direct time-domain moment method, which is applicable to arbitrarily shaped models made of conductors and dielectrics. Using the method, we have analysed the cross talk phenomenon within a LSI package. They demonstrated that in the PCB with the LSI and a cable, the noise induced by the cross talk causes the strong radiation through the cable.Sheldon et al [22] presented an efficient method of minimizing the area of power/ground (P/G) networks in integrated circuit layouts subjected to the reliability constraints. Researcher depicted that their developed model is fast enough that P/G networks with more than one million branches that might be sized in a few minutes on modern SUN workstations. Sudo et al [23] stated that electromagnetic interference (EMI) issues are expected to be crucial for next-generation system-on-package (SOP) integrated high-performance digital LSIs and for radio frequency (RF) and analog circuits.

Kurokawa et al [24] stated that recently deep submicron VLSI design, signal integrity (SI) and power-ground integrity (PGI) have become very important to design in a short time. To deal with such circumstances, authors proposed an approach called DEPOGIT, which is a new dense power-ground interconnect architecture that realizes more robust physical design integrity. Their quantitative analysis using 90 nm technology node, illustrated that high-quality decap of over 50 nF in a 10 mm square chip can be obtained, the resistive IR-drop can be less than 20% of that of a conventional power grid, transient peak noise can be reduced by about 80%, and the inductive crosstalk effect of the signal wire can be greatly reduced. Jingjing et al [25] presented an efficient method to simultaneously size wire widths and decoupling capacitance (decaps) areas for optimizing power/ ground (P/G) networks modelled as RLC linear networks subject to reliability constraints. Researchers stated such issues as a nonlinear optimization problem and proposed an efficient gradient-based non-linear programming method for searching the solution. They implemented a time-domain merged adjoint network for estimating the gradients efficiently and developed a novel equivalent circuit modeling technique to speed up the optimization process. Steinecke et al [26] stated that rising EMI potential of high-performance digital circuits like 32 bit microcontrollers demands for switching current models and feasible ways to run net list-based EMI simulations and thus considering this need, the researchers developed a

modeling approach for digital VLSI circuits and a silicon test vehicle to explore the correlation between models .Palit et al [27] developed a new, flexible and a very accurate crosstalk fault model that considered the capacitive coupling noise between the aggressor and the victim interconnect in deep sub-micron chips. Their proposed crosstalk model was on the basis of the distributed ABCD model of a long on-chip interconnect and takes into account the CMOS driver and receiver parameters of both aggressor and victim interconnects, besides the consideration of usual distributed per-unit-length RLGC parasitic elements and coupling capacitance, and interconnects length. Simulations were carried out using the Philips CMOS12 (130nm) technology parameters and the model accuracy was found very much close to PSPICE simulation result. Researchers stated that their proposed model can further be utilized to analyse/estimate the influence of interconnect parasitic on various signal integrity losses such as delay, glitch, overshoot, or crosstalk hazards. Mehrdad et al [28] presented a new automatic pattern generation methodology to stimulate the maximum power supply noise in deep submicron CMOS circuits. Our ATPG-based approach first generates the required patterns to cover 0 1 and 1 0 transitions on each node of internal circuitry.

Later, they applied a greedy heuristic to find the worst-case (maximum) instantaneous current and stimulate maximum switching activity inside the circuit. Their results depicted that the pattern pair generated by this approach produces a tight lower bound on the maximum power supply noise. Lin et al [29] also focused on the key issue of IR-drop in chips. Researchers criticized previous works as they might deal with only with power/ground (P/G) network peak current reduction to reduce the IR-drop problem only focus on synchronous sequential logic circuits which consider the combinational parts as unchangeable. However, some large combinational circuits which work alone in one clock cycle can create large current peaks and induce considerable IR-drops in the P/G network. Taking into consideration of these factors, in their researchers they proposed a novel combinational circuit IR-drop reduction methodology using Switching Current Redistribution (SCR) method. A novel combinational circuit partitioning method was proposed to rearrange the switching current in different sub-blocks in order to reduce the current peak in the P/G network, while circuit function and performance are maintained. Mohamood et al [30] proposed a new dynamic inductive-noise controlling mechanism at the micro architectural level that limit the on-die current demand within predefined bounds, regardless of the native power and current characteristics of running applications.. As compared to the other conventional systems, researchers stated that their di/dt controller is the first that takes the processor's floor plan as well as its power-pin distribution into account to provide a finer-grained control with minimal performance degradation. Jeffrey et al [31] proposed a novel on-chip voltage drop reduction technique for on-chip power delivery networks of VLSI systems in the presence of variational leakage current sources. They proposed the insertion of decoupling capacitors (decaps) into the power grid networks to reduce the voltage fluctuation and optimized their system based on sensitivity-based conjugate gradient method and sequence of linear programming approach. constant variations for different decap configurations of power grid circuits to speed up the statistical optimization process.

Zhong et al [32] stated that because of the positive feedback loop between power grid Joule heating and the linear temperature dependence of resistivity, non-uniform temperature profiles on the power grid in high-performance IC influence the IR drop in the power grid. Lack of accurate evaluation of thermal effect on the IR drop in the power grid may lead to over-design; or worse, underestimates the IR drop due to increased local temperature. Researchers in their work presented a method to compute the temperature-dependent IR drop on the power grid extremely fast. Further, they proposed a novel thermal model and a mathematical formulation to compute the temperature profiles on the power grid efficiently. Kohei et al [33] advised that this is the matter of fact that the test data modification based on test relaxation and X-filling is the preferable approach for reducing excessive IR-drop in at-speed scan testing to avoid test-induced yield loss, and existing test relaxation methods could not control the distribution of identified don't care bits (X-bits), thus adversely affecting the effectiveness of IR-drop reduction. Considering it as motivation, researchers proposed a novel test relaxation method, called Distribution-Controlling X-Identification (DC-XID), which intended to control the distribution of X-bits identified from a set of fully-specified test vectors for the purpose of effectively reducing IR-drop. Bronckers et al [34**]** proposed an approach that facilitates designers the necessary insight to solve this substrate noise issues. Their proposed methodology combined the strengths of the electromagnetic simulator, the parasitic extractor, and the circuit simulator that does not need doping profiles that are hard to get hold off. Their proposed methodology was demonstrated on two challenging examples:, in a 0.13-mum and a 90-nm CMOS technology. The substrate noise coupling mechanisms were revealed for both examples in a simulation time of less than 2 hours. Simulation results for their proposed system successfully validated on real-life prototypes of those examples with an accuracy of 1-2 dB. Vishweshwara et al [35] discussed in their research that design closure for predictable silicon performance is emerging as the most challenging digital VLSI design problem in advanced deep-submicron technology nodes. One of the significant problems is effective power-grid distribution, and the comprehension of the impact of voltage drops in the power grid on design timing and performance. Desouki et al [36] discussed that achieving power- and area-efficient fully integrated transceivers is one of the major challenges. Authors stated that the power losses associated with the parasitic of on-chip inductors, transistors, and interconnections have posed design challenges in the full integration of power-efficient CMOS radio-frequency integrated circuits (RF ICs). The layouts of the presented CMOS amplifiers were designed by carefully modeling the interconnection wires during the simulations and optimizing their widths for minimum

parasitic effects and hence optimum measured circuit performance. It exhibited a good match between the measured and simulated performance characteristics. Junxia et al[37] stated that as technology scales below 45nm and circuit integration density increases, power distribution network (PDN) contributes significantly to the total chip yield, escape, and reliability.A vector pair is generated to increase the region switching activity so that the gates will experience a larger-than-threshold IR-drop which may cause a timing or logic failure if only an open defect exists on power vias or power lines in that region. Various open defects on power/ground lines and vias are inserted and their impacts on circuit performance are investigated. They introduced a region sorting procedure in the proposed flow so as to reduce the computing effort. Healy et al [38] emphasized their research on 3-D integration for power supply network that may potentially increase performance and decrease energy consumption. By exploiting the smaller size and much higher interconnect density possible with TSVs they demonstrated significant reduction of nearly 50% in the IR-drop and 42% in the dynamic noise of our large-scale 3-D design. Through simulations, they also exhibited that a 3-tier stack with the distributed TSV topology actually lowers IR-drop by 21% and dynamic noise by 32% over a non-3-D system with less power dissipation. Rao et al [39] explored various reasons for variations in the power-distribution network which are exacerbated because of scaled supply voltages and smaller noise margins in sub-nanometer designs that adversely affect performance and yield. Researchers proposed a convolution-based dynamic method to estimate both IR and Ldi/dt drop on small combinational and sequential circuits and exhibited that the effectiveness of the design partitioning technique makes the framework feasible for a larger design.

III. STATUS OF THE WORK

The miniaturization of the integrated circuits (ICs) has caused reduction in size and highly compactness that enables functions even with reduced power consumption. But on contrary, it is giving rise to the cross talk complexity in source of EM interference at high frequency that ultimately degrades the performance of device ‘or’ chip.

We proposed a new technique to reduce the Electromagnetic interference and IR drop effects at high frequency. The effects of inductance and capacitance are lead to degrade the performance of the high speed integrated chip, In order to accomplish an optimal solution for aforementioned issues, in this research the Diagonal power routing has been implemented in top power layer (M9) that reduces the resistance and Inductance effect compared to the orthogonal power grid. Here in the proposed research model, the effects of chip temperature, electro migration and interconnect technology scaling have been considered for analysis. In fact, the voltage drop effect in the power/ground (P/G) distribution network increases swiftly as per technology scaling, and that using well-known countermeasures such as wire-sizing and/or decoupling capacitor insertion. Such approaches are in general employed in the current design methodologies which are of course insufficient to limit the voltage fluctuations over the power grid for next generation applications and future technologies. The voltage drops on power supply lines of switching devices in a clock distribution network that might introduce significant amount of skew which in turn degrades the signal integrity. Hence, in this work , the flop array method, swapping cell and clock buffers moments have been incorporated to reduce the IR drop.

IV .CONCLUSION

In this paper, various strategies and methodologies for reduction in electromagnetic interference and IR drop issues has been discussed .The impact of electromagnetic induction and electron migration on the IR drop and voltage drop in high speed VLSI design have been studied. A number of issues representing design constructs in high speed VLSI devices, varied proposed measures such as decap, structural modification etc have been discussed. The prime objective of this section is to facilitate the research objective oriented discussion for the existing literatures and their respective strengths as well as limitations etc. Taking into consideration of the significances of the theoretical understanding of the intended research domain of the electromagnetic interferences in high speed VLSI devices is discussed.

REFERENCES

[1] Yi-Min Jiang; Kwang-Ting Cheng, "Analysis of performance impact caused by power supply noise in deep submicron devices," Design Automation Conference, 1999. Proceedings. 36th , vol., no., pp.760,765, 1999

[2] Sinha, A.; Chowdhury, S., "Mesh-structured on-chip power/ground: design for minimum inductance and characterization for fast R, L extraction," Custom Integrated Circuits, 1999. Proceedings of the IEEE 1999 , vol., no., pp.461,465, 1999

[3] Cui, W.; Li, M.; Luo, X.; Drewniak, J.L.; Hubing, T.H.; VanDoren, T.P.; Du Broff, R.E., "Anticipating EMI from coupling between high-speed digital and I/O lines," Electromagnetic Compatibility, 1999 IEEE International Symposium on , vol.1, no., pp.189,194 vol.1, 1999

[4] Wei Cui; Xiaoning Ye; Archambeault, B.; White, D.; Min Li; Drewniak, J.L., "EMI resulting from signal via transitions through the DC power bus," Electromagnetic Compatibility, 2000. IEEE International Symposium on , vol.2, no., pp.821,826 vol.2, 2000

[5] Zheng, L.-R.; Tenhunen, H., "Effective power and ground distribution scheme for deep submicron high speed VLSI circuits," Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on , vol.1, no., pp.537,540 vol.1, Jul 1999

[6] Kimothi, S.K.; Nandwani, U.K., "Uncertainty considerations in compliance-testing for electromagnetic interference," Reliability and Maintainability Symposium, 1999. Proceedings. Annual , vol., no., pp.265,268, 18 -21 Jan 1999

[7] Shiyou Zhao; Roy, K., "Estimation of switching noise on power supply lines in deep sub-micron CMOS circuits," VLSI Design, 2000. Thirteenth International Conference on , vol., no., pp.168,173, 2000

[8] Resve Saleh, Syed Zakir Hussain, Steffen Rochel, Memberand David Overhauser, “Clock Skew Verification in the Presence of IR-Drop in the Power Distribution Network” IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 19, NO. 6, JUNE 2000

[9] Sasaki, H.; Harada, T.; Kuriyama, T., "A new VLSI decoupling circuit for suppressing radiated emissions from multilayer printed circuit boards," Electromagnetic Compatibility, 2000. IEEE International Symposium on, vol.1, no., pp.157, 162 vol.1, 2000

[10] Wei Cui; Xiaoning Ye; Archambeault, B.; White, D.; Min Li; Drewniak, J.L., "EMI resulting from a signal via transition through DC power bus-effectiveness of focal SMT decoupling," Environmental Electromagnetics, 2000. CEEM 2000. Proceedings. Asia-Pacific Conference on , vol., no., pp.91,95, 2000

[11] Steinecke, T., "Design-in for EMC on CMOS large-scale integrated circuits," Electromagnetic Compatibility, 2001. EMC. 2001 IEEE International Symposium on, vol.2, no., pp.910, 915 vol.2, 2001

[12] Steinecke, T.; John, W.; Koehne, H.; Schmidt, M., "EMC modeling and simulation on chiplevel," Electromagnetic Compatibility, 2001. EMC. 2001 IEEE International Symposium on , vol.2, no., pp.1191,1196 vol.2, 2001

[13] Kevin T. Tang and Eby G. Friedman, **"**Simultaneous Switching Noise in On-Chip CMOS Power Distribution Networks**"** IEEE April 16, 2000; revised January 20, 2001.

[14] Li Chen, Xiaoliang Bai, and Sujit Dey "Testing for Interconnect Crosstalk Defects Using On-Chip Embedded Processor Cores" DAC 2001, June 18-22, 2001, Las Vegas, Nevada, USA.

[15] M. Nourani, A. Attarha. "Signal Integrity: Fault Modeling and Testing in High-Speed SoCs". Journal of Electronic Testing: Theory and Applications (JETTA), 2002, pp. 539-554.

[16] Premkishore Shivakumar Michael Kistler "Modeling the Effect of Technology Trends on the Soft Error Rate of Combinational Logic" Appears in the Proceedings of the 2002 International Conference on Dependable Systems and Networks

[17] Shiyou Zhao; Roy, K.; Cheng-Kok Koh, "Power supply noise aware floorplanning and decoupling capacitance placement," Design Automation Conference, 2002. Proceedings of ASP-DAC 2002. 7th Asia and South Pacific and the 15th International Conference on VLSI Design. Proceedings. , vol., no., pp.489,495, 2002

[18] Kao, J.T.; Miyazaki, M.; Chandrakasan, A.P., "A 175-MV multiply-accumulate unit using an adaptive supply voltage and body bias architecture," Solid-State Circuits, IEEE Journal of, vol.37, no.11, pp.1545, 1554, Nov 2002

[19] Grochowski, E.; Ayers, D.; Tiwari, V., "Microarchitectural simulation and control of di/dt-induced power supply voltage variation," High-Performance Computer Architecture, 2002. Proceedings. Eighth International Symposium on , vol., no., pp.7,16, 2-6 Feb. 2002

[20] Harada, T.; Sasaki, H.; Kuriyama, T., "Radiated emission from a multilayer PCB with traces placed between power/ground planes," Electromagnetic Compatibility, 2002. EMC 2002. IEEE International Symposium on , vol.1, no., pp.253,257 vol.1, 19-23 Aug. 2002

[21] Ohtsu, S.; Nagase, K.; Yamagajou, T., "Analysis of radiation caused by LSI package cross talk and cable by using the time-domain moment method," Electromagnetic

[22] Sheldon X.-D. Tan, C.-J. Richard Shi, Senior "Efficient VLSI Power/Ground Network Sizing Based on Equivalent Circuit Modeling" IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL 22, NO. 3, MARCH 2003

[23] Sudo, T.; Sasaki, H.; Masuda, N.; Drewniak, J.L., "Electromagnetic interference (EMI) of system-on-package (SOP)," Advanced Packaging, IEEE Transactions on , vol.27, no.2, pp.304,314, May 2004

[24] Kurokawa, A.; Ono, N.; Kage, T.; Masuda, H., "DEPOGIT: dense power-ground interconnect architecture for physical design integrity," Design Automation Conference, 2004. Proceedings of the ASP-DAC 2004. Asia and South Pacific , vol., no., pp.517,522, 27-30 Jan. 2004

[25] Jingjing Fu, Zuying Luo, Xianlong Hong, Yici Cai, Sheldon X.-D. Tan, and Zhu Pan "Simultaneous Wire Sizing and Decoupling Capacitance Budgeting for Robust On-Chip Power Delivery" PATMOS 2004, LNCS 3254, pp. 433–441, 2004.

[26] T Steinecke, Koehne, M Schmidt "Behavioral EMI models of complex digital VLSI circuits" Microelectronics Journal Volume 35, Issue 6, June 2004, Pages 547–555, 3rd International workshop on Electromagnetic compatibility of Integrated circuits

[27] Palit, A.K.; Lei Wu; Duganapalli, K.K.; Anheier, W.; Schloeffel, J., "A New, Flexible and Very Accurate Crosstalk Fault Model to Analyze the Effects of Coupling Noise between the Interconnects on Signal Integrity Losses in Deep Submicron Chips," Test Symposium, 2005. Proceedings. 14th Asian , vol., no., pp.22,27, 18-21 Dec. 2005

[28] Mehrdad Nourani, Mohammad Tehranipoor, Nisar Ahmed "Pattern Generation and Estimation for Power Supply Noise Analysis" Proceedings of the 23rd IEEE VLSI Test Symposium (VTS'05)

[29] Hai Lin, Yu Wang, Rong Luo, Huazhong Yang, and Hui Wang "IR-drop Reduction through Combinational Circuit Partitioning" (Eds.): PATMOS 2006, LNCS 4148, pp. 370–381, 2006. c Springer-Verlag Berlin Heidelberg 2006

[30] Mohamood, F.; Healy, M.B.; Sung Kyu Lim; Lee, H.-H.S., "A Floorplan-Aware Dynamic Inductive Noise Controller for Reliable Processor Design," Microarchitecture, 2006. MICRO-39. 39th Annual IEEE/ACM International Symposium on , vol., no., pp.3,14, Dec. 2006

[31] Jeffrey Fan, Ning Mi, Sheldon X.-D. Tan "Voltage Drop Reduction for On-chip Power Delivery Considering Leakage Current Variations" 1-4244-1258-7/07/$25.00 ©2007 IEEE

[32] Yu Zhong; Wong, M.D.F., "Thermal-Aware IR Drop Analysis in Large Power Grid," Quality Electronic Design, 2008. ISQED 2008. 9th International Symposium on , vol., no., pp.194,199, 17-19 March 2008

[33] Kohei Miyase , Kenji Noda Hideaki Ito, Kazumi Hatayama, Takashi Aikyo, Yuta Yamato, Hiroshi Furukawa, Xiaoqing Wen , Seiji Kajihara "Effective IR-Drop Reduction in At-Speed Scan Testing Using Distribution-Controlling X-Identification" 978-1-4244-2820-5/08/$25.00 2008 IEEE

[34] Bronckers, S.; Scheir, K.; Van der Plas, G.; Vandersteen, Gerd; Rolain, Y., "A Methodology to Predict the Impact of Substrate Noise in Analog/RF Systems," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on , vol.28, no.11, pp.1613,1626, Nov. 2009

[35] Vishweshwara, R.; Venkatraman, R.; Udayakumar, H.; Arvind, N.V., "An Approach to Measure the Performance Impact of Dynamic Voltage Fluctuations Using Static Timing Analysis," VLSI Design, 2009 22nd International Conference on , vol., no., pp.519,524, 5-9 Jan. 2009

[36] El-Desouki, M.M.; Abdelsayed, S.M.; Deen, M.J.; Nikolova, N.K.; Haddara, Yaser M., "The Impact of On-Chip Interconnections on CMOS RF Integrated Circuits," Electron Devices, IEEE Transactions on, vol.56, no.9, pp.1882, 1890, Sept. 2009

[37] Junxia Ma, Mohammad Tehranipoor, Ozgur Sinanoglu and Sobeeh Almukhaizim "Identification of IR-drop Hot-spots in Defective Power Distribution Network Using TDF ATPG" 978-1-61284-292-9/10/$26.00 2010 IEEE

[38] Healy, M.B.; Sung Kyu Lim, "Distributed TSV Topology for 3-D Power-Supply Networks," Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , vol.20, no.11, pp.2066,2079, Nov. 2012

[39] Rao, Sushmita Kadiyala; Shivashankar, Bharath; Robucci, Ryan; Banerjee, Nilanjan; Patel, Chintan, "Scalability study of PSANDE: Power supply analysis for noise and delay estimation," VLSI Test Symposium (VTS), 2015 IEEE 33rd , vol., no., pp.1,6, 27-29 April 2015